## REMARKS

This is in response to the Office Action dated October 17, 2005. In that Office Action, Examiner rejected claims 1-18 (all the claims) under 35USC103(a) as being unpatentable over Blish, II US Patent 5,914,837 in view of Hu USP 5,938,769. In the Office Action, Examiner noted that: "Blish describes an array of voltage regulators (220a-220n) connected in parallel, and having a first voltage regulator that accepts a first power demand that is lower than the second power demands which would be greater. Blish discloses the claimed device except for having differing load power demand rates." (emphasis added). This conclusion appears to be based on Applicants' remarks in a prior amendment, following a rejection of claims based solely on Blish.

Examiner further states that: "Hu discloses that it is known in the art to provide a having differing load power demand rates. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide an array of voltage regulators (220a-220n) connected in parallel of Blish with the provide a having differing load power demand rates of Hu, in order to provide a more diversified and power supply system capable of handling load and power demands of the circuit."

Applicants disagree with the contention that Hu provides critical elements of applicants' invention that are suggested by neither Blish nor Hu. It is agreed that Hu teaches the concept of a microprocessor operating at different frequencies. In fact, he proposes toggle switches to select a range between 2 and 5.5 of the frequency multiplication factor of the CPU. (Abstract) In particular, "A fourth switch of the toggle switch member 70 is connected with a clock pin CLK ot the CPU 80 for setting the clock power of the CPU 80" (emphasis added). (column 3 lines 24-27) The power supply of Blish is certainly capable of providing a higher power level to the CPU of Hu when a greater load power is demanded by the CPU to operate at a higher frequency.

However, neither Blish nor Hu suggest the requirement for responding to a load power demand rate that would be different for the two different power levels. Thus, neither Blish nor Hu even remotely teach: second power regulators configured to respond to

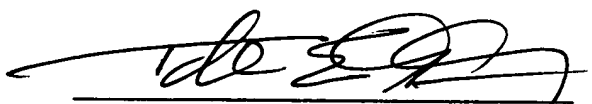
a load power demand rate greater than said first power regulator responds to power demands, as succinctly claimed by applicants.

As previously noted, since no mention in Blish is made to the contrary, it is presumed that all the regulators provide current to the microprocessor as well as the logic gates at the same speed. Similarly, there is no mention in Hu for demanding power at a different rate when the CPU frequency is increased. Neither Blish nor Hu are concerned with the speed with which currents are provided because a response to transient events is a problem not addressed in the CPU design of Hu or power supply design of Blish.

As also previously noted, Blish does not teach supplying power to a microelectronic device with second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands. Rather, Blish is limited to different load power demand levels by the microprocessor and logic gates. Hu is similarly concerned only with power demand levels as the CPU clock operating frequency is increased. Thus, the combination of two references where neither reference suggests applicants' invention cannot be said to properly raise a question of obviousness.

In view of the foregoing, it is believed that claims 1-18, all the claims currently in this application, are in condition for allowance. If Examiner has a question or comment or if Applicants' attorney can assist in any manner whatsoever, Examiner is respectfully requested to telephone the undersigned. An early notification of allowance is earnestly solicited.

Respectfully submitted,
William Pohlman et al



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